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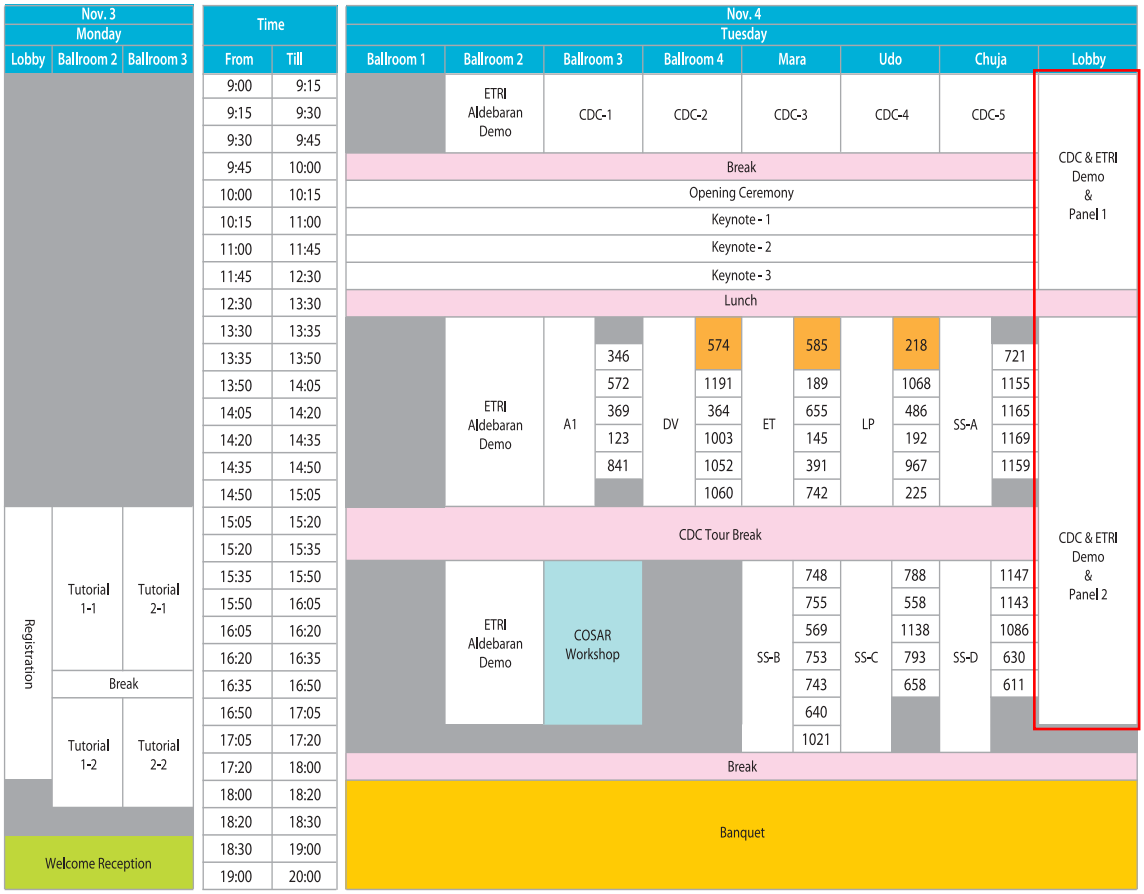
IEEE Catalog Number : CFP1469E-USB ISBN : 978-1-4799-5126-0

Time Table

Monday ~ Tuesday, November 3~4, 2014



A1 Analog and Mixed-Signal Techniques I
DV Digital Circuits and VLSI Architectures
ET Emerging technology
LP Power Electronics / Energy Harvesting Circuits
SS-A Invited Special Session: Near-Threshold Voltage Circuit Design
SS-B Invited Special Session: Image Signal Processing for Vision/Multimedia SoC
SS-C Invited Special Session: Analog/Digital Circuits for Mobile SoC
SS-D Invited Special Session: Design, Analysis and Tools for Integrated Circuits and Systems (DATICS)

Chulkyu Park, Seungheun Song, and Joongho Choi
University of Seoul, Korea

CDC(P)-154 SIMD Based Multi-Core Architecture for Real-Time Image Processing
Junsang Seo, Yonghun Park, Inkyu Jeoung, Myeongsu Kang, and Jong-Myon Kim
University of Ulsan, Korea

CDC(P)-155 All-Digital On-chip Process Sensor using Ratioed Inverter Based Ring Oscillator
Young-Jae An, Dong-Hoon Jung, Kryungho Ryu, and Seong-Ook Jung
Yonsei University, Korea

CDC(P)-156 An Implementation of Gbps level PHY Transmitter Using 65nm CMOS Technology
Hyunsub Kim and Jaeseok Kim
Yonsei University, Korea

CDC(P)-157 Optimized Intra Prediction for real-time HEVC Encoder
Youngjo Kim, Kyungmook Oh, and Jaeseok Kim
Yonsei University, Korea

CDC(P)-158 Fast-Lock Delay-Locked Loop Using Cyclic-Locking Loop with Duty-Cycle Correction for DRAM
Dong-Hoon Jung, Young-Jae An, Kyungho Ryu, Jung-Hyun Park, and Seong-Ook Jung
Yonsei University, Korea

CDC(P)-159 A bandwidth-tunable optical receiver
Kang-Yeob Park, Hyun-Yong Jung, and Woo-Young Choi
Yonsei University, Korea

CDC(P)-160 A Learning Neuromorphic IC Using Leakage Current
Hwa-Suk Cho, Byungsub Kim, Hong-June Park, and Jae-Yoon Sim
Pohang University of Science and Technology(POSTECH), Korea

CDC Demo Session

09:00~17:00 Lobby

Chair: Kwang Hyun Baek *(Chung-Ang University, Korea)*
Kyoung Rok Cho *(Chungbuk National University, Korea)*

CDC(D)-1 Design of the Floor Plane Removal System for Motion Recognition Using Depth Images
Geun-Jun Kim, Kyounghoon Jang, Hosang Cho, and Bongsoon Kang
Dong-A University, korea

CDC(D)-2 CMOS RF Energy Harvesting Rectifier using Parasitic Capacitance Compensation Technique and Low-Pass Filter
Junsik Park, Jaeyeon Kim, Seungwook Lee, Phirun Kim, and Yongchae Jeong
Chonbuk National University, korea

CDC(D)-3 A Protype for Estimating SoC in the Battery-powered the Mobile System
Minsu Oh and Hyunjin Kim

A bandwidth-tunable optical receiver

Kang-Yeob Park, Hyun-Yong Jung, and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University
Seodaemun-gu, Seoul 120-749, Korea
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I. INTRODUCTION

The optical receiver is one of the most critical components in optical links, and its performance can affect the whole optical interconnect system performance. Bandwidth, power consumption, transimpedance gain, and sensitivity are key design parameters for the optical receiver. The optimum bandwidth can be determined, considering tradeoffs between inter-symbol interference (ISI) and noise, 0.7 times the target bitrate [1]. Therefore, when a specific application requires changes in the target bitrate, the receiver should have the bandwidth-tuning capability. In this paper, we demonstrate an optical receiver that can tune its bandwidth for the target data rate range of 1Gbps to 13Gbps while maintaining transimpedance gain and power efficiency.

II. DESCRIPTION

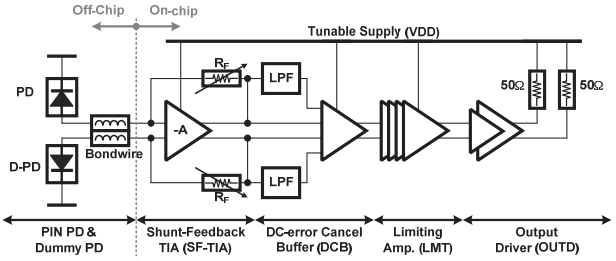

Fig. 1. Simplified block diagram of a tunable optical receiver.

To change the bandwidth of an optical receiver, a bandwidth-adjustable equalizer circuits can be adopted [2]. In this scheme, the bandwidth can be easily controlled by digitally switching parallel capacitor arrays. But it suffers from low power efficiency at the low speed, because it consumes constant power across the entire frequency range. In the shunt feedback scheme, a variable feedback resistor for conversion gain scaling can be adopted for the bandwidth control [3]. Because of tradeoffs between gain and bandwidth, the gain control provides the receiver bandwidth-tuning ability. But it also consumes a constant amount of power for both low- and high-speed operations. In order to solve this limitation, we design the tunable optical receiver having supply voltages scaled with the target bit rates. Fig. 1 shows the block diagram of our bandwidth-tunable optical receiver. It consists of shunt-feedback transimpedance amplifier (SF-TIA) with tunable feedback resistors, DC-offset-error cancellation buffer, limiting amplifier, and output driver.

In the shunt-feedback structure, the transimpedance gain and the bandwidth reduce as supply voltage scales down. By adding parallel resistor arrays with a digitally controlled switch as a feedback resistor (R_F), we can maintain the gain. 16 of 10-kΩ resistor arrays with NMOS switches are used for controlling the feedback resistance from 0.65kΩ to 10kΩ. A binary-to-thermometer conversion circuit is used to control the gain.

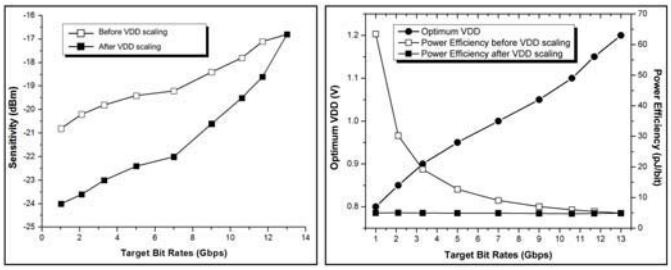

Fig. 2. Measured sensitivity and optimum supply voltage.

III. EXPERIMENT RESULTS

The receiver's 3-dB bandwidth is 0.76GHz at 0.8-V supply with 10-kΩ R_F and 9.05GHz at 1.2-V supply with 0.8-kΩ R_F, respectively. With this, the optimum operation range for the receiver is from 1 to 13Gbps. At 1-Gbps, the optical sensitivity for 10^{-12} BER is measured to -20.8dBm without any supply and R_F scaling. With bandwidth tuning, we can achieve -24.2dBm of sensitivity at 1Gbps. At 6.25-Gbps, we can obtain -22dBm of sensitivity, which is 2.8dB better than the non-tunable receiver, as shown in Fig. 2. At 13-Gbps, the optical receiver consumes 52.87mA at 1.2V corresponding 4.88pJ/bit. This increases up to 63.44pJ/bit at 1Gbps without any scaling. However, with scaling, we achieve less than 5pJ/bit.

ACKNOWLEDGEMENT

The authors would like to thank the IC Design Education Center (IDEC), Korea, for EDA software support and chip fabrication.

REFERENCE

[1] C. Hermans and M. S. J. Steyaert, "A high-speed 850-nm optical receiver front-end in 0.18-um CMOS," IEEE J. Solid-State Circuits, vol. 41, no. 7, pp. 1606-1614, Jul. 2006.

[2] J.-S. Youn, M.-J. Lee, K. Park, H. Rucker, and W.-Y. Choi, "A bandwidth adjustable integrated optical receiver with an on-chip silicon avalanche photodetector," IEICE Electronics Express, vol. 8, no. 7, pp. 404-409, Apr. 2011.

[3] H.-Y. Hwang, J.-C. Chien, T.-Y. Chen, and L.-H. Lu, "A CMOS tunable transimpedance amplifier," IEEE Microwave and Wireless Components Letter, vol. 16, no. 12, pp. 693-695, Dec. 2006.

11th International SoC Design Conference 2014
Chip Design Contest, CDC(P)-159, #201402168

A Bandwidth-Tunable Optical Receiver with Supply Voltage Scaling

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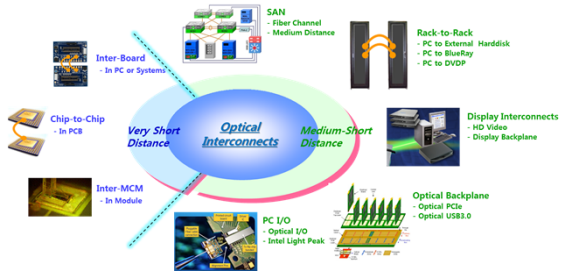
Introduction

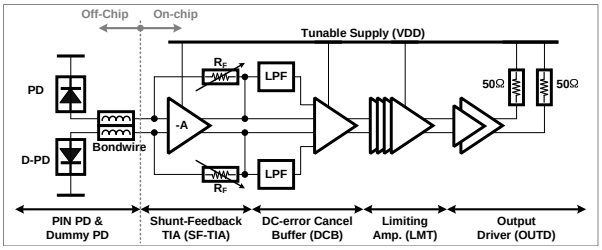


- ✓ Optical interconnects have broadened their applications from long-haul interconnects to short-reach applications.

- ✓ There are various interconnect standards requiring **various data rates.**
- ✓ Optical receiver is one of the most critical components in optical links, and its performance can affect the entire optical interconnect system performance.
- ✓ Bandwidth, power consumption, transimpedance gain, and sensitivity are key parameters in the optical receiver.
- ✓ The optimum receiver bandwidth is determined by the target data rates.
- ✓ **When the target data rate changes, the optical receiver should change its bandwidth. Consequently, bandwidth tuning capability is required.**
- ✓ We demonstrate a bandwidth-tunable optical receiver in the range from 1Gbps to 13Gbps using the supply voltage scaling technique while maintaining transimpedance gain and power efficiency.

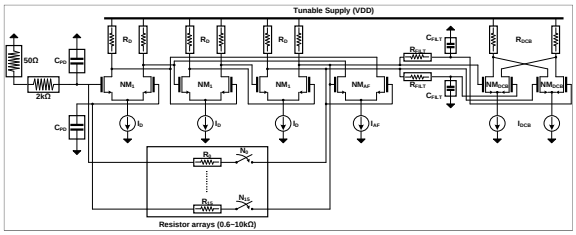
Bandwidth-tunable optical receiver design using voltage scaling

Block diagram of tunable TIA



- ✓ Shunt-feedback TIA w/ tunable feedback resistors (R_F)
- ✓ DC-offset-error cancellation buffer
- ✓ Limiting amplifier and output driver

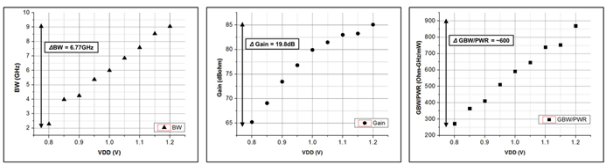
Tunable TIA Schematic



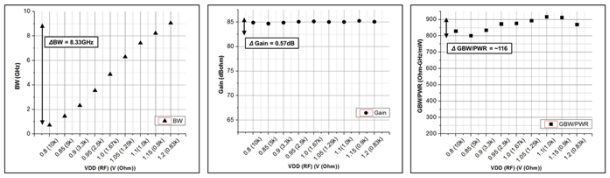
- ✓ TIA 3-dB bandwidth is controlled with supply voltage scaling.
- ✓ Tunable feedback resistor maintains the transimpedance gain even with voltage scaling.

Measurement setup

<Bandwidth, gain, and GBW/PWR as a function of VDD>



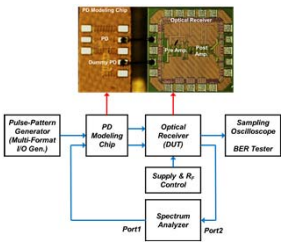
<Bandwidth, gain, and GBW/PWR as a function of VDD & R_F>



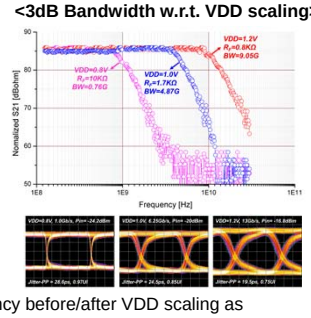
- ✓ GBW/PWR : Gain-bandwidth product per power consumption
- ✓ By controlling VDD along with R_F, constant gain and GBW/PWR is achieved

Measurement results

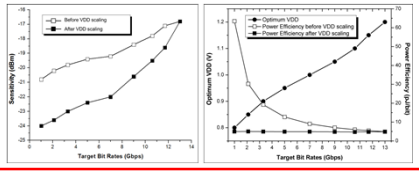
<Chip photo and measurement setup>



<3dB Bandwidth w.r.t. VDD scaling>



- ✓ Measured Sensitivity & Power efficiency before/after VDD scaling as function of target bit rates



Conclusion

- ❖ A bandwidth-tunable optical receiver is demonstrated in standard 65-nm CMOS technology
- ❖ With simple controls of supply voltages and feedback resistances of the receiver, 8.29-GHz bandwidth tuning range is achieved while maintaining the power efficiency and transimpedance gain.
- ❖ This bandwidth-tuning ability allows the optical receiver to have the best sensitivity and the power efficiency for various bit rates.